

**What is claimed is:**

1. A circuit for generating a clock signal, comprising:

a phase comparator for detecting a difference between a predetermined input clock signal and feedback of an output clock signal, and generating a shift control signal;

a phase control signal generator for receiving the input clock signal and generating the phase control signal according to the shift control signal using a predetermined clock generating reference signal;

a clock signal generator for receiving the phase control signal and generating an output clock signal having a frequency corresponding to a plurality times the frequency of the input clock signal.

2. The circuit for generating the clock signal in claim 1, wherein the phase comparator outputs a shift control signal commanding a left shift when the phase of the output clock signal is faster than that of the input clock signal and outputs a shift control signal commanding a right shift when the phase of the output signal is slower than the that of the input clock signal.

3. The circuit for generating the clock signal in claim 1, wherein the phase comparator comprises:

a shift register for storing a predetermined reference signal beforehand and shifting the clock generating reference signal according to the shift control signal;

a synchronized signal providing part connected to the shift register for synchronizing the shifted clock generating reference signal;

a plurality of delay loop connected to the synchronized signal providing part for generating a plurality of phase control signal by delaying set time according to the shifted location of the clock generating reference signal.

4. The circuit for generating the clock signal in claim 3, wherein the shift register stores high phase clock generating reference signals to an output terminal and all of low phase clock generating signals to the rest of the output terminals.

5. The circuit for generating the clock signal in claim 3, wherein each of the plurality of delay loops comprises a plurality of delays for delaying the clock generating reference signals for 'n' (a natural number) times longer than a preset time period.

6. The circuit for generating the clock signal in claim 5, wherein the preset time is set according to the clock generating reference signals outputted from the synchronized signal providing part.

7. The circuit for generating the clock signal in claim 1, wherein the clock signal generator comprises:

a plurality of correction delay for delaying the phase control signal for a time period according to the predetermined set time;

a pulse signal generator for generating a predetermined pulse signal according to the delayed phase control signal;

a clock signal outputting part for outputting output the output clock signal according to the pulse signal.

8. The circuit for generating the clock signal in claim 7, wherein each of the plurality of correction delays receives and delays the phase control signals on the basis of required time from generating the pulse signals at the plurality of pulse signal generators to generating output clock signals.

9. The circuit for generating the clock signal in claim 7, wherein the plurality of pulse signal generator comprises:

a plurality of first inverters for inverting and delaying for a preset time the delayed phase control signal and a phase control signal not delayed;

a NAND gate for inverting and logical-multiplying the delayed phase control signal and the output signals from the plurality of inverters;

a second inverter for inverting output signals from the NAND gate.

10. The circuit for generating the clock signal in claim 7, wherein the clock signal generator comprises:

a PMOS transistor and an NMOS transistor connected in series between an outlet and a grounding;

a plurality of third inverters connected to a connection point of the PMOS transistor and the NMOS transistor for working by latch;

a fourth inverter connected to the latch for inverting input signals.

11. The circuit for generating the clock signal in claim 10, wherein PMOS transistor gate is connected to the output terminal of the plurality of pulse signal generators through a first NOR gate and the NMOS transistor gate through a second NOR gate and a fifth inverter.